Marco Donato, Ph.D. May 2020

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RESEARCH INTERESTS

Methodologies for energy-efficient and reliable hardware systems targeting emerging computing paradigms. Design of embedded non-volatile memory subsystems with applications to machine learning hardware accelerator SoCs. Modeling and analysis of intrinsic noise sources in nanoscale circuits.

EDUCATION

2016 **Ph.D. in Electrical Sciences and Computer Engineering**, Brown University, Providence, RI, USA.
Thesis: Noise Modeling and Simulation Frameworks for the Design of Subthreshold Ultimate CMOS Circuits
Faculty Advisor: R. Iris Bahar, Professor of Computer Science and Electrical Engineering

2010 **M.Sc. in Electrical Engineering**, Università di Roma La Sapienza, Rome, Italy.

2008 **B.Sc. in Electrical Engineering**, Università di Roma La Sapienza, Rome, Italy.

ACADEMIC EXPERIENCE

2020 – **Research Associate in Electrical Engineering and Computer Science**
School of Engineering and Applied Sciences, Harvard University, Cambridge, MA

2017-19 **Postdoctoral Fellow in Electrical Engineering and Computer Science**
School of Engineering and Applied Sciences, Harvard University, Cambridge, MA
Faculty Mentor: Gu-Yeon Wei, Professor of Electrical Engineering and Computer Science

2017-18 **Lecturer in Electrical Engineering**
School of Engineering and Applied Sciences, Harvard University, Cambridge, MA

2016-17 **Postdoctoral Research Associate in Electrical Engineering**
School of Engineering, Brown University, Providence, RI
Faculty Mentor: R. Iris Bahar, Professor of Computer Science and Electrical Engineering

PUBLICATIONS

2020 G. Ko, Y. Chai, **M. Donato**, P. Whatmough, T. Tambe, R. Rutenbar, D. Brooks, G.-Y. Wei, "A 3mm^2 Programmable Bayesian Inference Accelerator for Unsupervised Machine Perception using Parallel Gibbs Sampling in 16nm" in *IEEE Symposium on VLSI Circuits* (VLSIC)

E. Rezaei, **M. Donato**, W. Patterson, A. Zaslavsky, and R. I. Bahar, "Fundamental Thermal Limits on Data Retention in Low-Voltage CMOS Latches and SRAM" *IEEE Transactions on Device and Materials Reliability*

P. Whatmough. **M. Donato**, G. Ko, S.K. Lee, D. Brooks, and G.-Y. Wei, "CHIPKIT: An agile, reusable open-source framework for rapid test chip development", *IEEE Micro*

2019 **M. Donato**, L. Pentecost, D. Brooks, and G.-Y. Wei, "MEMTI: Optimizing on-chip non-volatile storage for visual multi-task inference at the edge", *IEEE Micro*

L. Pentecost, **M. Donato**, B. Reagen, U. Gupta, S. Ma, G.-Y. Wei, and D. Brooks, "MaxNVM: Maximizing DNN storage density and inference efficiency with sparse encoding and error mitigation" in *Proceedings of the 52th Annual IEEE/ACM International Symposium on Microarchitecture* (MICRO)

S. Ma, **M. Donato**, S. K. Lee, D. Brooks, and G.-Y. Wei, "Fully-CMOS multi-level embedded non-volatile memory devices with reliable long-term retention for efficient storage of neural network weights", *IEEE Electron Device Letters*

U. Gupta, B. Reagen, L. Pentecost, **M. Donato**, T. Tambe, A. Rush, G.-Y. Wei, D. Brooks, "MASR: A modular accelerator for sparse RNNs", in *Proceedings of the 27th International Conference on Parallel Architectures and Compilation Techniques* (PACT) **Best Paper Nomination**

E. Rezaei, **M. Donato**, W. Patterson, A. Zaslavsky, and R. I. Bahar, "Thermal noise-induced error simulation framework for subthreshold CMOS SRAM" in *2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference* (S3S)

P. Whatmough, S. K. Lee, **M. Donato**, H. C. Hsueh, S. Xi, U. Gupta, L. Pentecost, G. Ko, D. Brooks, and G.-Y. Wei, "A 16nm 25mm^2 SoC with a 54.5x flexibility-efficiency range from dual-core Arm Cortex-A53, to eFPGA, and cache-coherent accelerators" in *IEEE Symposium on VLSI Circuits* (VLSIC)

2018 **M. Donato**, B. Reagen, L. Pentecost, U. Gupta, D. Brooks, and G.-Y. Wei, "On-chip deep neural network storage with multi-level eNVM" in *Proceedings of the 55th Annual Design Automation Conference* (DAC)

M. Donato, R. I. Bahar, W. R. Patterson, and A. Zaslavsky, "A sub-threshold noise transient simulator based on integrated random telegraph and thermal noise modeling" *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*

2016 **M. Donato**, R. I. Bahar, W. Patterson, and A. Zaslavsky, "A fast simulator for the analysis of sub-threshold thermal noise transients" in *Proceedings of the 53rd Annual Design Automation Conference* (DAC)

X. Han, **M. Donato**, R. I. Bahar, W. Patterson, and A. Zaslavsky, "Design of error-resilient logic gates with reinforcement using implications" in *Proceedings of the 26th Edition on the Great Lakes Symposium on VLSI* (GLSVLSI)

2015 **M. Donato**, R. I. Bahar, W. Patterson, and A. Zaslavsky, "A simulation framework for analyzing transient effects due to thermal noise in sub-threshold circuits" in *Proceedings of the 25th Edition on Great Lakes Symposium on VLSI* (GLSVLSI)

2012 **M. Donato**, F. Cremona, W. Jin, R. I. Bahar, W. Patterson, A. Zaslavsky, and J. Mundy, "A noise-immune sub-threshold circuit design based on selective use of Schmitt-trigger logic" in *Proceedings of the 22th Edition on Great Lakes Symposium on VLSI* (GLSVLSI)

P. Jannaty, F. C. Sabou, S. T. Le, **M. Donato**, R. I. Bahar, W. Patterson, J. Mundy, and A. Zaslavsky, "Shot-noise-induced failure in nanoscale flip-flops Part I: Numerical framework" *IEEE Transactions on Electron Devices*

P. Jannaty, F. C. Sabou, S. T. Le, **M. Donato**, R. I. Bahar, W. Patterson, J. Mundy, and A. Zaslavsky, "Shot-noise-induced failure in nanoscale flip-flops Part II: Failure rates in 10-nm ultimate CMOS" *IEEE Transactions on Electron Devices*

PRESENTATIONS

Tutorials

2020 **CHIPKIT: 2nd Tutorial on Agile Research Test Chips**
International Symposium on Computer Architecture (ISCA)

2019 **CHIPKIT - Tutorial on Agile Research Test Chips**
International Symposium on Microarchitecture (MICRO), Columbus, OH

Invited Talks

2019 **Optimizing non-volatile storage for energy-efficient inference at the edge**
University of Virginia, Charlottesville, VA

2018 **ASCENT (Applications and Systems-driven Center for Energy-Efficient integrated Nano Technologies) Review**
University of Michigan, Ann Arbor, MI

Co-design of Neural Network Weights and eNVM Encoding for On-Chip Storage
Auburn University, Auburn, AL, USA

2016 **Noise Modeling and Simulation Frameworks for the Design of Sub-threshold Ultimate CMOS Circuits**
Johns Hopkins University, Baltimore, MD
Harvard University, Cambridge, MA

Workshops

2016 **Modeling, Simulation Frameworks and Noise-immune Design of Sub-threshold Ultimate CMOS Circuits**
ACM/SIGDA Ph.D. Forum, Austin, TX

2015 **A Fast Simulator for the Analysis of Sub-Threshold Thermal Noise Transients**
8th IEEE/ACM Workshop on Variability Modeling and Characterization, Austin, TX

2011 **A Synthesis Tool for Designing Noise-Immune Circuits via Selectively Reinforced Logic**
SELSE-10, Stanford University, CA

Designing, Fabricating, and Testing Noise Immune Circuits
Subthreshold Microelectronics Conference, MIT Lincoln Laboratory, Lexington, MA

Noise-Tolerant Nanotransistor Circuitry
Rhode Island Nanotechnology Showcase, Providence, RI

Noise-Immune CMOS Circuits for Sub-Threshold Operation Using Schmitt-Trigger Logic
IEEE North Atlantic Test Workshop, Lowell, MA

TEACHING & ADVISING

Lecturer
Harvard University, Cambridge, MA
Circuits, Devices, and Transduction, Undergraduate Level (Fall 2018)
Electronic Devices and Circuits, Undergraduate Level (Fall 2017, Spring 2017)

Teaching Assistant
Brown University, Providence, RI
Design of Computing Systems, Undergraduate Level (Spring 2011, Spring 2015)
Design and Implementation of VLSI Systems, Undergraduate level (Spring 2013 — Fall 2014)
Reconfigurable Computing, Graduate level (Fall 2014)

Certifications
The Harriet W. Sheridan Center for Teaching and Learning, Brown University, Providence, RI, USA
Certificate I — Reflective Teaching in Higher Education (2014-2015)

Advising Experience
5 undergraduate students and 2 graduate students at Brown University (2012-17)
2 graduate students at Harvard University (2017-19)

FELLOWSHIPS & AWARDS

2018 SRC JUMP Applications Driving Architecture Center - Best paper Q2

2015 ACM Research Student Competition – Third Place

Brown University Doctoral Research Travel Grant

2014 Brown University Joukowsky Summer Research Award

2012 TiROP International Exchange Student Scholarship (Tokyo Institute of Technology)

2011 IEEE North Atlantic Test Workshop - Jake Karrafalt Best Student Paper Award

PROFESSIONAL SERVICE

Technical Program Committee Experience
International Conference on Computer Aided Design (ICCAD)
Design Automation Conference (DAC)
International Symposium on Low Power Electronics and Design (ISLPED)
International Conference on Very Large Scale Integration (VLSI-SoC)

Journal and Conference Review
IEEE Transactions on Circuits and Systems I & II

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
IEEE Computer Architecture Letters
IEEE Transactions on Very Large Scale Integration Systems
IEEE Transactions on Nanotechnology
IEEE Design & Test
IEEE Transactions on Magnetics
Elsevier Integration: The VLSI Journal
IEEE International Symposium on Circuits and Systems (ISCAS)
Midwest Symposium on Circuits and Systems (MWCAS)